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... Synopsys, Synchronous (Dual Clock) **FIFO** Controller with ... Synopsys, Embedded Memory **BIST** Controller Core. ... Implementation, DW_sqrt_seq, Synopsys, **Sequential** SquareRoot ...
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On the Identification of Optimal Cellular Automata for Built-In ...

... Paolo (1996) (Correct) 0.2: Cellular Automata for Deterministic **Sequential** Test.. ...
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... memory minimum readout rate of 10 MW/s (**sequential**). ... and B memories can be independently
 commanded for **BIST**. ... and is synchronized and buffered in a small **FIFO**. ...
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... Combinational circuit: 0.0267 μ W/MHz/gate **Sequential** circuit: 0.0215 ... 10-bit x
 128-word **FIFO** SRAM Four ... Embedded test circuits SCAN, BSCAN, **BIST**, TestBus Notes ...
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MJ LeVine

... an initial address and a data register implement **sequential** access to ... was a data
 overrun in the **FIFO** during the ... with a built-in self test (**BIST**), allowing it ...
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... Separate data **FIFO** fills with long **sequential** writes. ... 3) Improving Test Coverage •
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... of building blocks, such as SRAMs, **FIFO** structures, random ... techniques developed for improving **BIST** capabilities of ... In **sequential** circuits, a sizable number of ...

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